

What is claimed is:

1. A digital data driver, comprising:
a plurality of data lines, each transferring first data during a first period and second data during a second period;
a first shift register outputting a first enable signal during the first period;
a second shift register outputting a second enable signal during the second period; and
a plurality of transmission controllers coupled to the a plurality of data lines respectively, each having first to fourth latches and a first inverter;
wherein each transmission controller stores the first data and the second data in the second latch and the first latch respectively according to the first enable signal and the second enable signal; each transmission controller outputs the first data stored in the second latch to the fourth latch and outputs to a DAC according to a third enable signal; each transmission controller outputs the second data stored in the first latch to the third latch and outputs to a second DAC through the first inverter according to a fourth enable signal.

2. The digital data driver as claimed in claim 1, wherein the transmission controller further comprises:
parallel first and second switching devices, each having a first terminal coupled to one of the data lines

5 and a second terminal coupled to an input terminal
6 of the first latch;
7 parallel third and fourth switching devices, each having
8 a first terminal coupled to an output terminal of
9 the first latch and a second terminal coupled to
10 an input terminal of the second latch;
11 parallel fifth and sixth switching devices, each having
12 a first terminal coupled to an output terminal of
13 the second latch and a second terminal coupled to
14 an input terminal of the third latch; and
15 a seventh switching device having a first terminal
16 coupled to an output terminal of the third latch
17 and a second terminal coupled to an input terminal
18 of the fourth latch, wherein the first inverter has
19 an input terminal coupled to the output terminal
20 of the third latch.

1 3. The digital data driver as claimed in claim 2,
2 wherein the first and third switching devices are turned on
3 to store the first data in the second latch according to the
4 first enable signal, the second switching device is turned
5 on to store the second data in the first switching device
6 according to the second enable signal, the fifth switching
7 device and the seventh switching device are turned on to output
8 the first data to the first DAC according to the third enable
9 signal, and the fourth switching device and the sixth
10 switching device are turned on to output the second data to
11 the second DAC through the first inverter according to the
12 fourth enable signal.

1 4. The digital data driver as claimed in claim 2,
2 wherein the first to seventh switching devices are
3 transmission gates.

1 5. The digital data driver as claimed in claim 2,
2 wherein the first to seventh switching devices are switching
3 transistors.

1 6. The digital data driver as claimed in claim 2,
2 wherein the third enable signal and the fourth enable signal
3 are produced in a third period and a fourth period in a blanking
4 period, wherein the third enable signal controls the fifth
5 switching device and the seventh switching device, the fourth
6 enable signal controls the fourth switching device and the
7 sixth switching device.

1 7. A liquid crystal display, comprising:
2 a plurality of pixels arranged in a matrix;
3 a scan driver turning on each row of pixels arranged in
4 the matrix sequentially; and
5 a digital data driver outputting data to the
6 corresponding pixels, each comprising:
7 a plurality of data lines, each transferring first
8 data during a first period and second data
9 during a second period;
10 a first shift register outputting a first enable
11 signal during the first period;
12 a second shift register outputting a second enable
13 signal during the second period; and
14 a plurality of transmission controllers coupled to
15 a plurality of data lines respectively, each

16 having first to fourth latches and a first
17 inverter; wherein each transmission
18 controller stores the first data and the
19 second data in the second latch and the first
20 latch respectively according to the first
21 enable signal and the second enable signal;
22 each transmission controller outputs the
23 first data stored in the second latch to the
24 fourth latch and outputs to a DAC according
25 to a third enable signal; each transmission
26 controller outputs the second data stored in
27 the first latch to the third latch and outputs
28 to a second DAC through the first inverter
29 according to a fourth enable signal.

1 8. The liquid crystal display as claimed in Claim 7,
2 wherein the transmission controller further comprises:
3 parallel first and second switching devices, each having
4 a first terminal coupled to one of the data lines
5 and a second terminal coupled to an input terminal
6 of the first latch;
7 parallel third and fourth switching devices, each having
8 a first terminal coupled to an output terminal of
9 the first latch and a second terminal coupled to
10 an input terminal of the second latch;
11 parallel fifth and sixth switching devices, each having
12 a first terminal coupled to an output terminal of
13 the second latch and a second terminal coupled
14 to an input terminal of the third latch; and

15 a seventh switching device having a first terminal
16 coupled to an output terminal of the third latch
17 and a second terminal coupled to an input terminal
18 of the fourth latch, wherein the first inverter has
19 an input terminal coupled to the output terminal
20 of the third latch.

1 9. The liquid crystal display as claimed in claim 8,
2 wherein the first and third switching devices are turned on
3 to store the first data in the second latch according to the
4 first enable signal, the second switching device is turned
5 on to store the second data in the first switching device
6 according to the second enable signal, the fifth switching
7 device and the seventh switching device are turned on to output
8 the first data to the first DAC according to the third enable
9 signal, and the fourth switching device and the sixth
10 switching device are turned on to output the second data to
11 the second DAC through the first inverter according to the
12 fourth enable signal.

1 10. The liquid crystal display as claimed in claim 8,
2 wherein the first to seventh switching devices are
3 transmission gates.

1 11. The liquid crystal display as claimed in claim 8,
2 wherein the first to seventh switching devices are switching
3 transistors.

1 12. The liquid crystal display as claimed in claim 8,
2 wherein the third enable signal and the fourth enable signal
3 are produced in a third period and a fourth period during a
4 blanking period, wherein the third enable signal controls the

5 fifth switching device and the seventh switching device, the
6 fourth enable signal controls the fourth switching device and
7 the sixth switching device.

1 13. The liquid crystal display as claimed in claim 9,
2 wherein the first DAC and second DAC convert the first data
3 and the second data into a first analog data and a second analog
4 data and output to corresponding pixels respectively after
5 receiving the first data and the second data.